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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,299	11/05/1999	JAMES A. JOHANSON	JOHANSON79-3	3784

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FARKAS & MANELLI PLLC
2000 M STREET N W 7TH FLOOR
WASHINGTON, DC 200363307

EXAMINER	
ANYA, CHARLES E	

ART UNIT	PAPER NUMBER
2126	10

DATE MAILED: 08/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/434,299	JOHANSON ET AL.	
	Examiner	Art Unit	
	Charles E Anya	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3/ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5, 802, 351 to Frampton in view U.S. Pat. No. 5,537,576 to Perets et al. and further in view of Feemster et al.

As to claim 1, Frampton teaches a Shared Memory (Dual Random Access Memory Device 31, Col. 3, Ln. 18 – 26), a First Processor (MCU System 21, Col. 3, Ln. 18 – 26), a Second Processor (DSP System 22, Col. 3, Ln. 18 – 26), a First Mailbox Portion (Figure 4, MCU to DSP ---→ Zero to Size – 1, Col. 5, Ln. 35 – 38), a Second Mailbox Portion (Figure 4, DSP to MCU --→ Size to Last, Col. 5, Ln. 35 – 38), a Low Physical Address End (Zero, Col. 5, Ln. 35 – 38), a High Physical Address (Size – 1, Col. 5, Ln. 35 – 38) and having write access to the first mailbox portion (Col. 8, Ln. 1 – 17).

Frampton do not explicitly teach filling downward toward the low physical address and the first processor as not having access to the second mailbox portion.

Perets teaches filling downward toward the low physical address (Col. 6, Ln. 32 – 41, Col. 8, Ln. 40 – 52).

Feemster teaches the first processor as not having access to the second mailbox portion (Col. 4, Ln. 4 – 16). It would have been obvious to improve upon the system of taught by Frampton by implementing the improvements detailed above because it would provide the system taught by Frampton with the enhanced capability of reduced latency, overhead and eliminate concern about overwriting information (Col. 4, Ln. 30 – 45).

As to claim 2, Frampton teaches second processor as having access to the second mailbox portion (Col. 7, Ln. 4 – 9).

Frampton does not explicitly teach the second processor as not having access to the second mailbox portion.

Feemster teaches the first processor as not having access to the second mailbox portion (Col. 4, Ln. 4 – 16). It would have been obvious to improve upon the system of taught by Frampton by implementing the improvements detailed above because it would provide the system taught by Frampton with the enhanced capability of reduced latency, overhead and eliminate concern about overwriting information (Col. 4, Ln. 24 – 45).

As to claim to 3, Frampton teaches the first processor as having read access to the first mailbox (Col. 6, Ln. 41 – 45).

Frampton is silent with reference to the first processor having read access to the second mailbox portion.

Feemster teaches a first processor that has read access to the second mailbox portion (Col. 4, Ln. 17 – 23). It would have been obvious to improve upon the system taught by

Frampton by implementing the improvements detailed above because it would provide the system of Frampton with the enhanced capability of eliminating latency (Col. 5, Ln. 1 – 11).

As to claim 4, claim 3 meets claim 4 except for the second processor having read access to the second mailbox portion.

Frampton is silent with reference to the second processor having read access to the second mailbox portion.

Feemster teaches a second processor that has read access to the second mailbox portion (Col. 4, Ln. 1 – 16). It would have been obvious to improve upon the system taught by Frampton by implementing the improvements detailed above because it would provide the system of Frampton with the enhanced capability of eliminating latency (Col. 5, Ln. 1 – 11).

As to claim 5, Frampton teaches a Dual Port Random Access Memory (Dual Port Random Access Memory Device 31, Col. 18 – 21).

As to claim 6, see the rejection of claims 1 and 3.

As to claim 7, see the rejection of claims 2 and 4.

As to claim 8, see the rejection of claim 1.

As to claim 9, Frampton teaches a Minimum Length (Zero, Col. 5, Ln. 9 – 24).

As to claim 10, Frampton teaches a Minimum Length (Size, Col. 5, Ln. 30 – 38).

As to claim 11, Frampton teaches reallocating a portion of a minimum length of the first physical address end (Col. 5, Ln. 30 – 36).

As to claim 12, Frampton teaches reallocating a portion of a minimum length of the second physical address end (Col. 5, Ln. 30 – 36). Also see the rejection of claim 1.

As to claim 13, see the rejection of claim 1.

As to claim 14, see the rejection of claim 9.

As to claim 15, see the rejection of claim 10.

As to claim 16, see the rejection of claim 11.

As to claim 17, see the rejection of claim 12.

Response to Arguments

2. Applicant's arguments filed 6/2/03 have been fully considered but they are not persuasive.

Applicant argues that it is improper to combine the Framptom and Perets prior art references.

Firstly, the Framptom prior art reference is the primary reference used for this rejection and the Perets prior art reference is used in conjunction to show the idea of having a shared memory grow /fill towards a common boundary from the top and bottom of the memory bank.

The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference rather the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.

Applicant's argues that figure 2 of Perets does not teach the first memory bank 14 as growing/filling from FFFF(hex) towards the bottom (line 36) and the second memory bank 15 as growing/filling from 0 towards the top (line 37).

The Examiner maintains that the first memory bank 14 grows/fills from FFFF(hex) towards FE00(hex) (line 36) and that the second memory bank 15 grows/fills from 0 towards 0CFF(hex) (line 37). This fact is made evident in column 6 lines 29 – 40. Here the first memory bank 14 (address line 18) starts from FFFF(hex) and **decrements** by one to FFFE(hex) while the second memory bank 15 **increments** by one from address 0 to 1. This implies that the first memory bank 14 grows towards the middle of the memory space 35 from FFFF(hex) and the second memory bank 15 grows to the middle of the memory space 35 from 0. If these were not correct as per the suggestion of the Applicant the Examiner would like to know why the Perets reference would be decrementing and incrementing towards the unallocated memory space and what would be explanation for the memory space between the lines 36 and 37 of figure 2.

Figure 8 further supports the Examiner's point that the first memory bank 14 and second memory bank 15 grows/fills from FFFF(hex) downwards and from 0 upwards respectively. Again here the first memory bank 14 is offset by –1 up to –400(hex) that is FFFF(hex) is decremented 1 as you move towards the common boundary or move away from FFFF(hex) and the second memory bank 15 is incremented from 0 up to 3FF(hex).

Also, the Perets reference in it's abstract teaches that the expansion or contraction of the memory banks is effected relative to a common boundary between the two memory

banks. This is to say that the common boundary is a factor or determinant of how the memory space expands or contracts, which goes to make Examiner's point that by having unallocated memory space as the common boundary the memory banks grows/fills towards this unallocated memory space and the size of this unallocated memory space determines how much the memory banks can grow/expand.

Please note that the Perets reference teaches address space 35 as a contiguous block of memory (The Abstract and Col. 8 Ln. 18 – 29).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles E Anya whose telephone number is (703) 305-3411. The examiner can normally be reached on M – F (First Friday off) from 8:30 am to 5:30 pm.

The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Charles E Anya
Examiner
Art Unit 2126